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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
PERT, EVAN T

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 08/30/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/652,216	JIANG ET AL.	
	Examin r	Art Unit	
	Evan T. Pert	2829	

-- The MAILING DATE of this communication appears on the cover she t with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30 and 66-104* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30 and 66-104* is/are rejected.

7)☒ Claim(s) *92 and 94* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *21 March 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The proposed correction to Fig. 4 was received on 3-21-02. The proposed correction is approved.

Claim Objections

2. Claims 92 and 94 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. In claim 66 from which claim 92 depends, the recited "device" *is* "a memory device" such that defining the device as "a memory device" in claim 92 does not further limit parent claim 66. Regarding claim 94, the recited "device" of the system is a "memory device", wherein "all memory devices" are inherently types of "logic devices" absent evidence to the contrary. Applicant is required to cancel or amend claims 92 and 94.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 66-104 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention:

Non-substrate area - In claim 96, "at least one non-substrate area of said device" is unclear. At line 2 of the claim, applicant recites "substrate" to mean what is typically called a semiconductor "die" or "chip" wherein the "substrate" of a "semiconductor device" is typically thought of as a supporting structure of the chip or die.

For purposes of examination, "non-substrate area" in the claim is taken to mean "not on the semiconductor substrate (of line 2 of the claim)".

Layer - The scope of meaning of the term "layer" throughout the claims is unclear. The *plain meaning* of "a layer" is "an extent of homogenous material with thickness", but applicant causes confusion by seemingly designating a layer as including a laminate of distinct conventional "layers" and "films" of differing composition and thickness [e.g. see claim 22 where the "layer comprises a film."]. For purposes of examination, applicant's claim term "layer" is interpreted to include laminates of films and sub-layers, in the broadest sense.

Conductive - The scope of the meaning of the term "conductive" is unclear since it could mean any of "electrically conductive" or "thermally conductive" or "electrically and thermally conductive." For purposes of examination, in view of applicant's *written description*, the scope of the term "conductive" in the claims is *limited* to "electrically conductive" [see lines 12-14 of page 10 of the specification, for example].

Film - The scope of the meaning of the term "film" in the claims is unclear. The term "film" is taken to mean "a thin layer", but the term "film" is a relative term without definition, making the term in this case indistinguishable from "layer". For purposes of examination, the term "film" is taken to mean a "thin layer", wherein all "layers" in semiconductor devices are reasonably thought of as "films" when they are *thin* compared to the substrate. However, the term "film" is indefinite in this case since the thickness at which "a film" becomes "a layer" is not defined.

Regions...receiving...voltage - The scope of meaning of "bias voltage distribution regions...receiving a bias voltage" throughout the claims is unclear as applicant does not set forth definitive scope in the *written description* of the specification. For purposes of examination, the term "bias voltage distribution regions" is taken to mean "regions where a potential of *any* biasing voltage is applied", wherein a "voltage" is inherently defined as a "difference in the electric potential between two points".

By the examiner's interpretation, when a "voltage is received at a region", one properly thinks of both electric potentials defining the voltage as being in "the region". However, applicant's use of "receiving a voltage" in "a region" particularly seems to mean the situation where only one potential defining the voltage is in "the region" with the second potential defining "the voltage" not in "the region".

Correction and/or explanation are required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 96 is rejected under 35 U.S.C. 102(b) as being anticipated by Osorio [U.S. Patent 5,317,107]:

Osorio discloses a "semiconductor device" 34 comprising: a "semiconductor substrate *die*" 46; at least one electrical element fabricated on said substrate die 46 [seen as "electrical connection of 50" at front side of semiconductor substrate die 46]; and a conductive layer 48 provided on a backside of said substrate die 46, said conductive layer 48 "forming an electrical path between said substrate die" 46 and at least "one non-substrate area of said device" [wherein the metal part 16 is a "non-substrate area" in view of the disclosure defining "semiconductor substrate" to mean the same thing as what is conventionally called a semiconductor "chip" or "die"].

6. Claims 1-3, 5, 8, 22, 29-30 and 97 are rejected under 35 U.S.C. 102(a) as being anticipated by Burr [U.S. Patent 6,048,746].

Regarding claims 1, 2 and 97, Burr discloses a "semiconductor device" that includes a plurality of "transistors" as in applicant's claim 2 (wherein each transistor is like the single transistor shown in Burr's Fig. 1 per col. 10, lines 34-42) comprising: a semiconductor substrate 105; at least one electrical element (i.e. the transistors) fabricated on an upper side of said substrate 105; *a plurality* of bias voltage distribution source regions 104 fabricated over said upper side of said substrate 105 for receiving a bias voltage V_{bs} and providing said bias voltage V_{bs} to said substrate [wherein Burr discloses "a plurality" of "distribution regions" 104 due to the "plurality of transistors" in the overall device]; and a conductive "metallic back plane" layer 106 wherein layer 106 "forms an electrical path (ohmic contact) between said substrate and said bias voltage source" [col. 1, line 55-56].

Regarding claim 3, the bias voltage V_{bs} is electrically coupled to "a terminal" [B in Fig. 1] supplying said bias potential V_b [wherein "potential" is inherently part of said "bias voltage" V_{bs} since the voltage V_{bs} is defined as the difference of electric potential $V_b - V_s$ = the "voltage" defined as V_{bs}. See col. 1, lines 54-57 teaching the control of potentials at S and B in Fig. 1 to establish bias voltage V_{bs} between "distribution source regions" 104 and at metallic back plane 106].

Regarding claim 5, layer 106 is inherently "a conductive metallic layer" since it is a "metallic back plane".

Regarding claim 8, "conductive metallic layer" 106 is "electrically coupled to a terminal supplying said bias voltage" V_{bs}. [See col. 1, lines 54-57].

Regarding claim 22, the layer 106 is considered as being a "film" since it is thin compared to substrate 105.

Regarding claims 29 and 30, a "processor device" inherently includes "logic devices" so a "processor" in itself is inherently a "logic device": Burr teaches that his inventive threshold voltage tuning with back biasing is applicable to "a typical microprocessor" [col. 4, line 41], which is a type of "processor" which is inherently a type of "logic device".

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Burr as applied to claim 1 above, and further in view of applicant's admitted prior art.

Burr does not disclose "plugs" for coupling, but applicant admits such plugs are "commonly provided" to couple bias voltage [page 1, lines 6-11].

It would have been obvious to one of ordinary skill in the art at the time of applicant's claimed invention to adopt plugs to reach distribution source regions 104 in Burr. One of ordinary skill in the art would have been motivated to adopt plugs where Burr shows a symbolic vertical line in order to achieve the required vertical electrical connection to the distribution source region 104. Applicant admits it is common to provide plugs to distribution regions so it is reasonable that one of ordinary skill in the art would readily adopt a "common" means to achieve the "required" vertical connection to distribution regions 104 in Burr.

9. Claims 98-99 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burr [U.S. Patent 6,048,746], as applied to claim 97 above, and further in view of Rodenbeck et al..

Burr does not disclose that the "electrical path" of claim 97 is formed when the backside metallic layer is "wire bonded to a bonding pad of the semiconductor device to form an electrical path to at least one area other than the area of the metallic layer" [as in claim 98] nor does Burr disclose that the "conductive layer" is in "electrical communication with a bonding pad of the semiconductor device" [as in claim 99].

That is, Burr does not disclose how the electrical connection of terminal "B" in Fig. 1 is to be carried out, but does indicate the supply for the connection is either "on the semiconductor device chip" [claims 8 and 17] or "off the chip" [claims 9 and 18].

Rodenbeck et al. teach a methodology that improves over wire bonding for back-side connection to a flip-chip wherein conductive material 20 cause "electrical communication" between a "bonding pad" of the chip and a back-side metal layer. Rodenbeck teaches that the prior art wire-bonding of the backside can be improved upon by using the conductive material 20 through a via or along side of the chip to reach "conventional bonding pads on the front side".

It would have been obvious to one of ordinary skill in the art at the time of applicant's claimed invention to adopt wire bonding or the improved method of Rodenbeck et al., motivated by a need to electrically connect terminal "B" of the backside metal layer 106 in Burr with the inherent bonding pad of its on-chip bias supply [Burr's claims 8 and 17]. One of ordinary skill could chose wire-bonding if that were the equipment available [Rodenbeck et al.; col. 2, lines 17-24] or might prefer to adopt Rudenbeck et al.'s material 20 for the "electrical communication" inherently required for Burr's on-chip supply to reach the backside metal biasing layer via terminal "B".

10. Claims 6-7, 9-17 and 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burr as applied to claim 1 above, and further in view of the "Intel 2000 Packaging Databoom" (Intel).

Burr does not disclose the particulars of metallic back plane metal layer 106. Instead, Burr relies on knowledge in possession of one of ordinary skill in the art at the time of his filing for making the metallic backside layer 106. For example, metallic conductive layers on the backside of semiconductor substrate die are taught as part packaging basics: Intel teaches that "some backside metal layers require electrical connection" just like the layer 106 in Burr requires electrical connection [Section 3.3.1 of Intel].

Regarding claim 7, Intel discloses that the metallic layer 106 in Burr can be advantageously attached with adhesive [Fig. 3-4 in view of row 2 of Table 3-2 of Intel].

Regarding claims 10, 11, 25 and 26, in view of rejections under 35 USC 112 for lack of clarity of a "film" and "layer", Fig. 3-1 of Intel discloses a "layer" which "includes" a "film" of "silver or gold" the "layer" being "on" the backside of the device substrate labeled "silicon".

Regarding claim 12, the "silver or gold" film in Fig. 3-1 in Intel, for example, is included as a "layer" and this "layer" clearly extends beyond the length of the silicon substrate.

Regarding claims 13, 16 and 17, Intel discloses conductive paste die attach as an option [3.3.2.3] wherein the silver-filled cured paste disclosed by Intel inherently has conductive silver particles in it.

It would have been obvious at the time of applicant's invention to recognize the advantage in performing die attach AND electrical connection as taught by Intel, as applied to the backside metal layer 106 in Burr, thus adopting any of the various die attach media and methodology disclosed by Intel for the varied expected advantages depicted by Table 3-2. One of ordinary skill in the art would have been motivated to adopt Intel "die attach media" for the express purposes of "attaching the chip" and for "making an electrical connection" as required in Burr [see paragraph beginning "Die attach media" in Section 3.3.1 of Intel].

Regarding claims 6, 9, 14, 15, 23, 24, Burr in view of Intel discloses the claimed invention except for the broadly claimed ranges of thickness and resistivity of the metallic layer on the backside of semiconductor substrate die. However, Intel does teach that the thickness [3.3.4.3] and resistivity are important (i.e. die attach materials are "electrically conductive"). The metal layers in both Intel and Burr inherently have a thickness and a resistivity. Choosing thickness and resistivity of the metal layer is a matter of appropriate design choice:

For example, it is notoriously well known to one of ordinary skill in the art that ideal resistivity of a perfect conductor is zero since any resistance creates electrical delay and I^2R losses.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to choose resistivity of the conductive backside die attach layer as close to zero as possible and to choose appropriate thickness of the metal layer such that a good ohmic contact is formed and so that the layer is thick enough for adequately securing the chip, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

11. Claims 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burr and Intel as applied to claims 13, 14, 15 and 17 above in view of Shah et al. (article entitled "Cyanate Ester Die Attach Material...") for teaching that the cured "Cynate Ester Ag-filled adhesive" depicted in Intel's Fig. 3-4 is an "isotropically conductive polymeric film" [abstract of Shah et al.]

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to adopt the polymeric film taught by Intel [Fig. 3-4] for the same reasons as adopting the "cured conductive paste" as is set forth in the rejection of claims 13, 14, 15 and 17 above.

12. Claims 100-104 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burr as applied to claims 1, 66 and 97-99 above, and further in view of Official Notice:

Burr does not disclose the limitation that the bias distribution regions *include* "an electrically conductive plug and a metallization layer."

The examiner takes *Official Notice* that notoriously well-known semiconductor device interconnect technology at the time of applicant's claimed invention included the deposition of "plugs" into openings of insulating layers to vertically reach electrical regions at the bottoms of the openings with an overlying patterned "metallization layer" provided for making lateral electrical connections [demonstrable by introductory textbooks, by patents and a variety of literature].

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to "include an electrically conductive plug and a metallization layer" with the claimed embodiments of claims 1, 66 and 97-99, motivated by the need to form 3-D electrical connections between electrical circuit nodes to render Burr's device operational.

13. Claims 27-28 and 66-95 are rejected under 35 USC 103: Claims 27, 28 and 66-68, 70, 73, 87, 94 and 95 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burr as applied to claims 1-3 above, and further in view of Houston. Claim 69 is rejected under 35 U.S.C. 103(a) as being unpatentable over Burr in view of AAPA as applied to claim 4 above, and further in view of Houston. Claims 71-72, 74-82 and 88-91 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burr in view of Intel as applied to claims 6-7, 9-17 and 23-26 above, and further in view of Houston. Claims 83-86 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burr in view of Intel taken with Shah et al., as applied to claims 18-21 above, and further in view of Houston.

Burr, Intel and AAPA do not disclose that the semiconductor device having the backside metal layer is advantageously a "memory device" of the "DRAM" type or a "processor" incorporated into a "processor system" with the memory device in communication with the processor, like in a computer pc.

However, Houston teaches that back biasing advantages are applicable to a DRAM memory device [col. 2] including ASICs and integrated processors [col. 10, lines 10-14].

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to adopt Burr's back biasing for tuning threshold voltages in a DRAM memory and/or processor taught by Houston. One of ordinary skill in the art would have been motivated to adopt the back-biasing structure with conductive metallic layer 106 as in Burr in order to achieve the expected advantage of lowering threshold voltages of DRAM memory logic processor devices disclosed by Houston [col. 4, lines 46-50 of Burr]. One of ordinary skill in the art would have been motivated to choose the particulars of a backside metal layer 106 in Burr in accordance with teachings of AAPA and Intel/Shah as is set forth in the rejections incorporated from above.

Response to Arguments

14. Applicant's arguments with respect to claims 1-99 have been considered but are moot in view of the new grounds of rejection. While applicant's arguments are moot in view of new rejections, the examiner would like to help clarify that applicant is mistaken in arguing that a backside metal layer added to admitted prior art is "novel because" applicant adds the metal layer for a "different reason" [pages 5-6 of paper no. 9].

Applicant is reminded that a proper rejection under 35 USC 103(a) does not require the obvious modification of a reference to be for "the same reason" as reasoned by applicant [MPEP 2144 section entitled "RATIONALE DIFFERENT FROM APPLICANT'S IS PERMISSIBLE"].

The reasons to add a metal layer to the backside of a semiconductor device substrate die (chip) in the prior art not only include "back biasing", but also include "die attach" and "heat sinking" (see Intel).

Applicant has argued, in paper no. 9, that the prior art fails to teach "the unique combination" of bias voltage distribution regions on a front side AND a metal layer on the backside (for biasing). However, the examiner does not understand applicant's reasoning that one of ordinary skill in the art would necessarily discard the use of a well known backside metal layer for "die attach" and "heat sinking" from applicant's admitted prior art front side biasing scheme, particularly when there is a clear "expected advantage" by adding a metal layer to the backside of the structure of any semiconductor substrate die.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Akram (U.S. Patent 6,064,116, commonly assigned with different inventive entity) is cited for teaching metal layers of solder, metal-filled epoxy and polyamide (polymeric) adhesive on the backside of semiconductor substrate die for optional back biasing, die attaching, and heat sinking.

Publication US 2002/0055246 A1 is cited for containing a duplicate of claims 1-30 and 66-99 in this case. Claims 1-30 and 66-99 have been cancelled from application serial number 09/998,165, with device claims 1-30 and 66-99 having been deemed patentably "distinct" from method claims 31-65 in paper no. 3 of the instant case.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan T. Pert whose telephone number is 703-306-5689. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 703-308-1680.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Evan Pert

ETP
August 28, 2002